Amendments of the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application.

Please amend claims 1, 3 – 11, and 13 - 17, inclusive, as follows:

Listing of Claims:

1 (Currently Amended). A digital processor responsive to a microinstruction to perform an operation, the digital processor comprising: ~~comprising,~~

a memory for storing data associated with the operation to be performed;

a finite state machine configuration circuit;

a configurable finite state machine coupled to the finite state machine configuration circuit, ~~(FSM)~~ the configurable finite state machine configurable to perform ~~for performing~~ a function in association with the operation; and

control circuitry for providing data to the memory ~~register~~ and for enabling execution of the FSM in response to detecting a predefined value in a field in the microinstruction. ~~microinstruction and for preventing execution of the FSM when the predefined value is not detected.~~

2 (Original). The digital processor of claim 1, further comprising loop control circuitry for repetitively accessing the data stored in the memory.

3 (Currently Amended). The digital processor of claim 1, wherein the control circuitry further comprises ~~includes ID~~ detection circuitry for determining that at least a portion of a microinstruction is to be implemented by the configurable finite state machine ~~FSM~~.

4 (Currently Amended). The digital processor of claim 1, further comprising a plurality of finite state machines, and ~~FSMs;~~

wherein the control circuitry further comprises: ~~includes~~

finite state machine ~~FSM~~ execution circuitry to selectively invoke operation of one or more of the plurality of finite state machines. ~~FSMs.~~

5 (Currently Amended). The digital processor of claim 1, ~~further comprising a configurable FSM; wherein the control circuitry includes~~ wherein the finite state machine configuration circuit further comprises ~~configuration~~ circuitry to direct the configurable finite state machine ~~FSM~~ to be configured in advance for a predetermined function associated with the microinstruction.

6 (Currently Amended). The digital processor of claim 1, wherein the memory further comprises ~~includes~~ a register.

7 (Currently Amended). The digital processor of claim 1, wherein the memory further comprises ~~includes~~ a microstore.

8 (Currently Amended). The digital processor of claim 1, wherein the memory further comprises ~~includes~~ a cache.

9 (Currently Amended). A computer processor for executing a microinstruction, the computer processor comprising: ~~comprising~~

a configurable finite state machine; ~~machine (FSM);~~

processing circuitry;

an iterative register; and

control circuitry for controlling the configurable finite state machine ~~FSM~~ and the iterative register to implement at least a portion of the microinstruction in parallel with the processing circuitry. ~~when a predefined value in a field in the microinstruction is detected and for preventing execution of the FSM when the predefined value is not detected.~~

10 (Currently Amended). The computer processor of claim 9, wherein the configurable finite state machine ~~FSM~~ and iterative register are operated concurrently.

11 (Currently Amended). A method for executing a microinstruction, the method comprising: ~~comprising~~

configuring a finite state machine to implement a first function indicated by the microinstruction;

using both **[[a]]** the finite state machine and an iterative register to perform ~~implement~~ at least a portion of **[[a]]** the first function indicated by the microinstruction; ~~and~~

allowing execution of the finite state machine if a predefined value in a field in the microinstruction is detected; and ~~detected and preventing execution of the finite state machine when the predefined value is not detected.~~

concurrently using processing circuitry to perform a second function indicated by the microinstruction.

12 (Previously Presented). The digital processor of claim 1, wherein the predefined value is represented by a single bit.

13 (Currently Amended). The digital processor of claim 12, claim 1, wherein a bit value of 0 prevents configurable finite state machine ~~FSM~~ execution, wherein a bit value of 1 enables configurable finite state machine ~~FSM~~ execution.

14 (Currently Amended). The digital processor of claim 1, wherein when configurable finite state machine ~~FSM~~ execution is enabled a predetermined field in the microinstruction is used to invoke configurable finite state machine ~~FSM~~ processing.

15 (Currently Amended). The digital processor of claim 14, wherein when configurable finite state machine ~~FSM~~ execution is prevented the predetermined field in the microinstruction is used for a purpose other than to invoke FSM processing.

16 (Currently Amended). The digital processor of claim 1, wherein multiple instructions are used for configurable finite state machine ~~FSM~~ control.

17 (Currently Amended). The digital processor of claim 16, wherein a predetermined field is used to indicate how many microinstructions are to be used for configurable finite state machine ~~FSM~~ control.